The PicoPak Clock Measurement Module

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• Keywords

Precise phase measurements, clock measurement module, frequency stability, direct digital synthesis, picoseconds, clock noise.

• Abstract

This paper describes a simple module for precise clock stability measurements based on the use of a direct digital synthesizer (DDS) as the means for making high-resolution phase measurements.

• Introduction

There is a continuing need for making precise clock stability measurements using inexpensive and easy-to-use hardware, and many techniques have been devised for doing so, including high resolution time interval counters (TIC), dual mixer time difference (DMTD) systems and, more recently, digital techniques similar to software defined radios (some using cross-correlation). This paper presents a new approach, suggested to the author by Mr. Tom Van Baak [1] at the 2014 PTTI meeting, which uses phase control of a direct digital synthesizer (DDS) in a microprocessor-controlled phase lock loop as a means for making moderately high resolution phase measurements. The technique compares the phase of the signal under test against a reference signal from the DDS at the same nominal frequency in an analog phase detector. The sense of the phase detector output is detected by an analog comparator whose 1-bit output steers the phase of the DDS via the microprocessor. Photographs of the PicoPak module are shown in Figures 1 and 2, and a block diagram of the basic system is shown in Figure 3.

Figure 1. Front of PicoPak Module

Figure 2. Rear of PicoPak Module

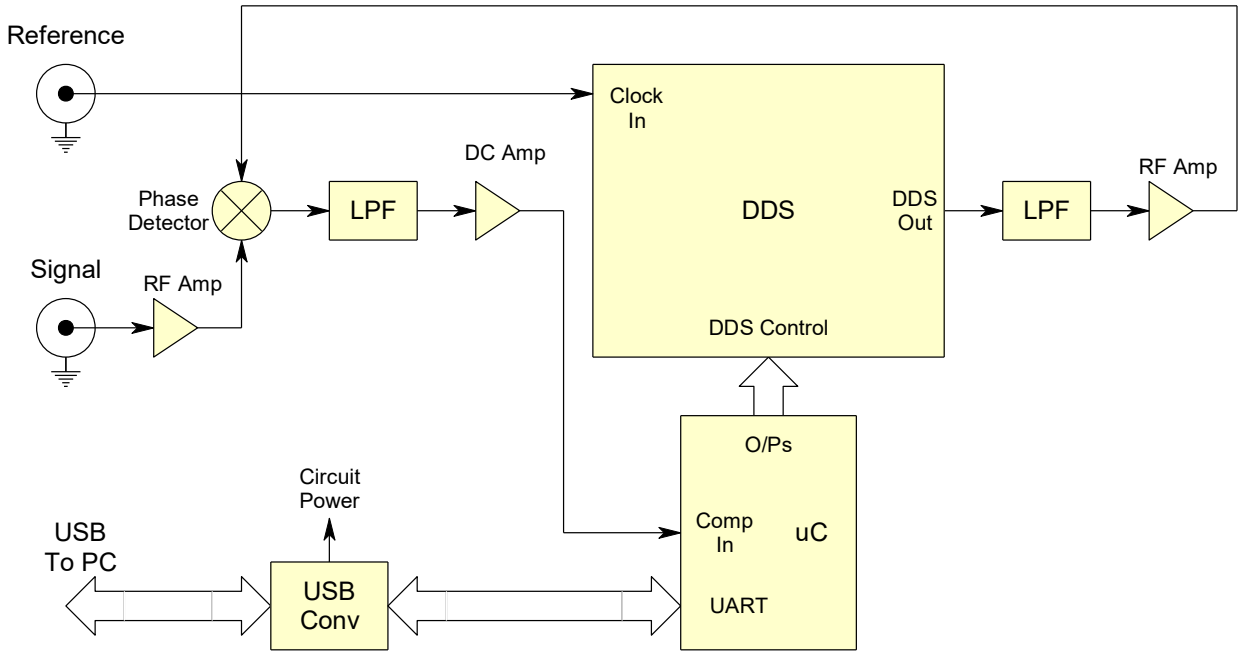


Figure 1. DDS Clock Measuring System Basic Block Diagram

The system is similar to a loose VCXO PLL used to demodulate phase variations [2]. In this case, the "loose PLL" is the means used to set the nominal DDS frequency. It also resembles the phase feedback circuit of Figure 6.15 of Reference 3. The phase tracking loop of the DDS clock measuring system keeps the phase detector centered at quadrature and uses the numeric DDS phase word to produce a phase data stream to the USB port.

At 10 MHz, a DDS chip with 14-bit phase control has a resolution of about 6.1 ps, which provides a quite useful measurement capability, a resolution of about $1x10^{-11}$ at 1 second and an 11-digit/s frequency counter. That resolution is adequate for measuring the vast majority of frequency sources (e.g., most crystal oscillators and atomic frequency standards). Furthermore, the resolution improves as tau at longer averaging times, e.g., $\approx 1x10^{-14}$ at 1000 seconds day down to a noise floor below $1x10^{-16}$ determined mainly by the thermal sensitivity of the phase detector.

The measuring system noise is dominated by white phase quantization noise; without any other noise contribution, one would expect the phase to alternate between two values separated by twice the DDS phase resolution as the +/- phase corrections are summed over a number of interrogation cycles [4]. The 12.2 ps peak-to-peak (6.1 ps rms) quantization and other noise sources (DDS, including its clock multiplier, RF buffer amplifiers, phase detector, DC amplifier, comparator, etc.) result in a typical coherent 1-second ADEV noise floor that is about $1.2x10^{-11}$[7].

Although the DDS phase measurement technique has somewhat limited phase resolution, it also has several advantages. Compared with phase interpolation, it does not require calibration, has no nonlinearity, and works as well at any relative phase condition without a dead zone. Compared with a dual mixer time difference clock measurement system, it does not depend on offset source noise cancellation, and its noise is independent of the phase difference between the reference and measurement signals. The incremental PicoPak phase measurements are relative to an arbitrary starting value of zero.

• **PicoPak Clock Measurement Hardware**

The basis of this clock measurement technique is a DDS chip with high-precision phase control, for example the Analog Devices AD9951 device used in the PicoPak module described herein [5]. A block diagram of the AD9951 is shown in Figure 2. The DDS works by incrementing its phase accumulator by the frequency word at each clock cycle, and the resulting phase value is transformed to a cosine function which is then converted to analog RF form by a DAC and low pass filter. For our purposes, the critical thing is that a 14-bit offset can be added to the phase value, thereby allowing the phase of the RF output to be adjusted. While this provides a very useful capability, it is interesting to note that even higher phase resolution (e.g., 0.2 ps) would be possible by expanding the width of the phase offset word to the full (e.g., 19-bit) width of the cosine conversion. That might be possible with a future DDS device or with one implemented by an FPGA or other custom logic device.

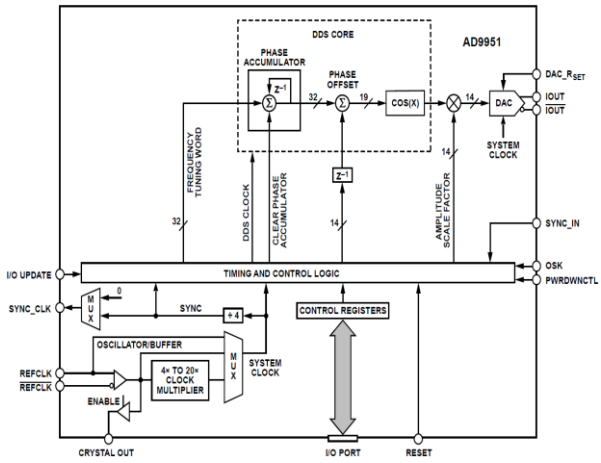


Figure 2. Block Diagram of the Analog Devices AD9951 DDS Chip

The finite 32-bit resolution of the DDS frequency adjustment is also a consideration because it introduces a frequency error on the reference signal compared with the nominal value of the signal under test. That causes the measured phase to have a (well-defined) ramp which must be mathematically removed from the raw measurements. For example, around 10 MHz, for a 32-bit DDS clocked at 120 MHz, the maximum frequency error is about 14 mHz or 1.4e-9; at exactly 10 MHz, the frequency offset is -9.31e-10, which corresponds to a phase slew of 931 ps/s or 153 DDS phase increments per second. That phase ramp has a period of about 107 seconds. An obvious way to improve this factor is to use a DDS with more frequency control bits (e.g., the 48-bit AD9852), but the effect of the residual frequency offset must be removed in any case. Means must also be provided to set the DDS frequency and acquire phase lock.

The phase resolution varies directly with the RF frequency; at 1 MHz it becomes x10 worse, 61 ps. One way to avoid that would be to use a higher DDS frequency and divide it down to the signal frequency. That works because the DDS phase increment is preserved through the divider. Toward higher frequencies, that method is limited by the frequency range of the DDS. For the AD9951, the resolution of a 10 MHz measurement could be improved by a factor of (say) x5 by clocking the DDS at its maximum 180 MHz and operating it at 50 MHz.

A Mini-Circuits SYPD-1 phase detector is used in the PicoPak module with nominal +7 dBm drive at its two RF ports. It has a sensitivity of 8 mV/degree, so 1 mV corresponds to 35 ps. The phase detector output is amplified by a factor of 11 before being applied to the comparator, thereby reducing the effect of

its hysteresis. The phase detector, op amp and comparator noise is not significant, and DDS phase jitter is the more important factor affecting the system noise floor.

The DDS is controlled by a small Microchip PIC16F1847 microcontroller [6]. That device has sufficient speed, program and RAM memory, I/O pins and functions (UART, comparators, ADCs, timers, etc.) for this application. Its main functions are to set the DDS frequency, acquire phase lock, track the phase detector variations using the DDS phase control and to communicate with a PC user interface application. A sampling rate of 2.5 kHz is used to interrogate the sense of the phase detector output, and 25 interrogation cycles are averaged to control the DDS phase and produce an optional 10 ms data stream. DDS frequency adjustments are made as required at a 100 ms rate, and the module produces composite phase, frequency adjustment and phase correction data via its user interface at a 1 second rate. The 2.5 kHz sampling rate is generated from the 10 MHz reference by another small PIC device programmed to serve as a x4000 divider.

- **PicoPak Clock Measurement Firmware**

The PIC16F1847 microcontroller firmware was written in C using the Microchip MPLAB X programming environment and its XC8 C compiler. The code implements a main loop that checks for commands from the USB interface while responding to periodic interrupts to perform the measurements, as shown in the flowchart of Figure 3.

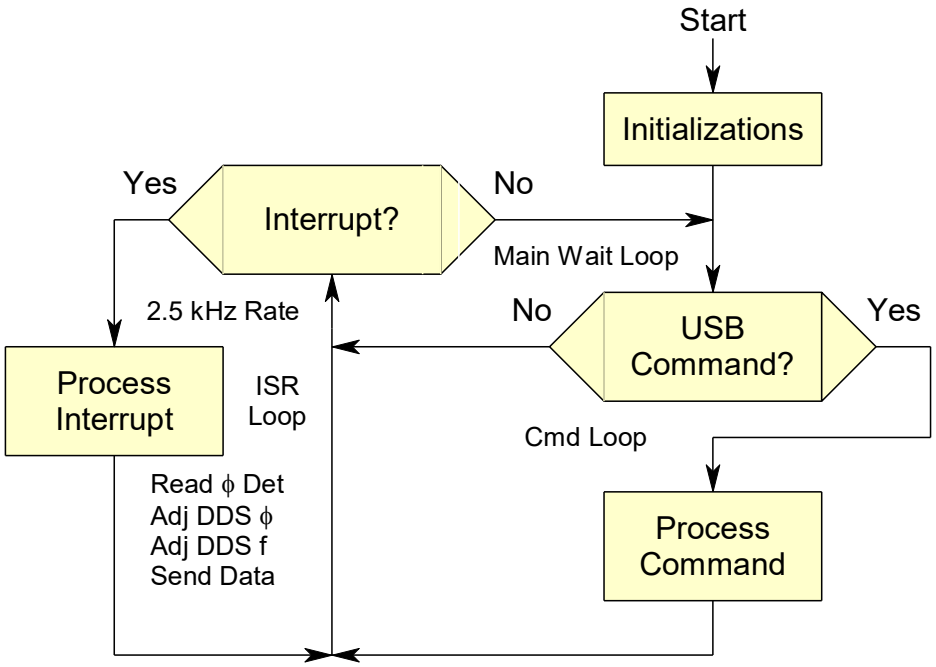


Figure 3. PicoPak Firmware Flowchart

The user interface commands are single ASCII letters as shown in Table I. Input commands are followed by any required data bytes in the form of ASCII hex characters from the PC, while output commands result in hex/byte characters being sent to the PC. The user interface can operate either via a terminal program or a complete graphical user interface.

The interrupt-driven measurements are divided into twenty-five 400 µs cycles, each able to perform an operation such as sending data to the DDS or USB interface within its time slot. The phase detector state

is sampled and the DDS phase is incremented or decremented accordingly at each interrupt cycle. These phase adjustments are summed over 25 cycles to produce an optional 10 ms data stream. The net phase adjustment over ten of those intervals is used to make any necessary frequency adjustments. Those phase and frequency adjustments, along with a phase correction for any frequency adjustments, are sent by the 1-second data stream.

Before the phase measurements can be made, it is necessary to set the DDS frequency close to that of the signal under test, and to acquire phase lock. The signal frequency is measured via a two-step process, first by making a 1-second frequency count, using that value to establish a beat note of about 100 Hz, and then making multiple single-period measurements to determine the signal frequency within a few pp10^9. That value is then used to set the DDS frequency close enough that the system will acquire phase lock, as indicated by a constant phase detector voltage at the center of its range (quadrature).

Table I PicoPak Clock Measurement Module Commands

Cmd	I/O	Description	Format	Remarks
A	Out	Read phase detector ADC	4 hex chars	mV=val·4096/1023
B	Out	Measure phase detector beat period	4 hex chars	T in units of 2X ref period (200 ns for 10 MHz) Expect C350 hex = 50,000 dec for 100 Hz beat note = 10 ms
C	Out	Read temperature	-	Not implemented
D	Out	Get DDS phase word	2 hex chars	Neither=00, Ref=01, Sig=10, Both (normal)=11
E	Out	Reference and signal check	4/2/2 hex chars	TMR1 O/Fs, TMR1H, TMR1L 1s counts
F	In	Enter DDS frequency word	8 hex chars	32-bit FTW0
G	-	Timing tests	-	For development testing only
H	Out	Measure signal frequency	4/2/2 hex chars	TMR1 O/Fs, TMR1H, TMR1L 1s counts Expect 989680 hex = 10,000,000 for 10 MHz
I	In	Enter freq adj step size	2 hex chars	1 through 3 allowed (01 – 03 hex)
J	Cmd	Increment DDS frequency	-	
K	Cmd	Decrement DDS frequency	-	
L	Cmd	Flash LED	-	
M	In	Enter DDS clock multiplier	2 hex chars	x4 to x12 = 04 to 14 hex
N	Out	Get module info	4/4/4 hex chars	Model, S/N & firmware version (factory cmd) e.g., 01, 64 & 1E hex = PP1, 100 & 0.30
O	Cmd	Toggle freq adjustments	-	Turn on/off frequency adjustments
P	In	Enter DDS phase word	4 hex chars	14-bit POW
Q	Cmd	Toggle I/O mode	-	Terminal or PC mode
R	Cmd	Reset PIC	-	No response in PC mode
S	Cmd	Toggle data stream #4	1 byte (char)	O/P is signed integer phase increment
T	Cmd	Toggle data stream #1	2 hex chars	O/P is signed integer phase increment
U	Cmd	Toggle data stream #2	2/2 hex chars	O/P is hex phase & frequency increments
V	In	Enter module info	4/4/4 hex chars	Model, S/N & firmware version
W	Out	Get DDS frequency word	8 hex chars	32-bit FTW0
X	Cmd	Go to PC I/O mode	-	All flags in reset state except I/O mode
Y	Cmd	Toggle data stream #3	4/2/2 hex chars	nPPPP, nFF and nCC, the phase increment, freq adjustment & phase correction counts
Z	Cmd	Zero the DDS phase	-	14-bit POW
<	Cmd	Lower PIC 32 MHz osc freq	-	Decrement OSCTUNE register TUN bits
>	Cmd	Raise PIC 32 MHz osc freq	-	Increment OSCTUNE register TUN bits

• DDS Clock Measurement Module User Interface Software

The clock measurement module PC user interface software was created using the Microsoft Visual C/C++ development environment. The user interface controls the measurement module, captures its data stream, displays the phase or frequency data, performs basic analysis and launches the Stable32 or TimeLab program for more extensive analysis. The main and configuration screens are shown in Figures 4 and 5.

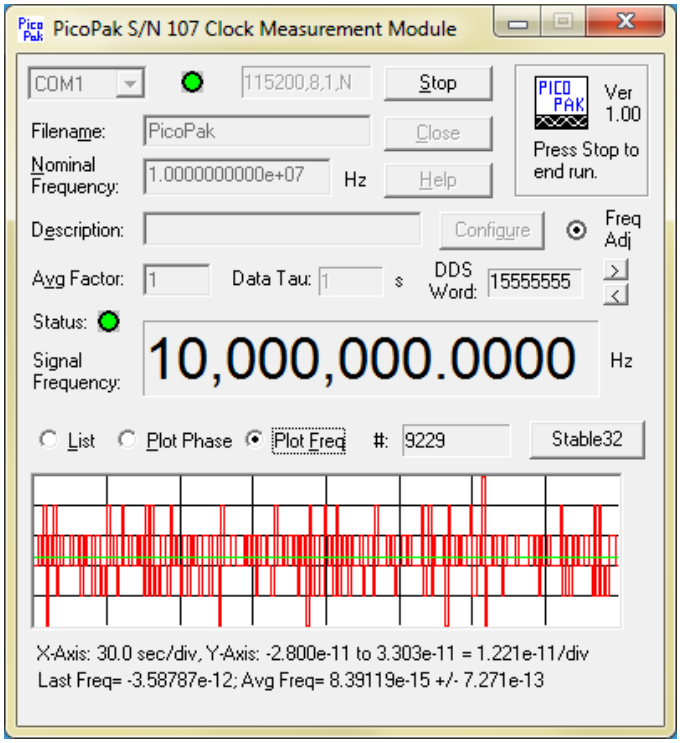


Figure 4. PicoPak User Interface Main Screen

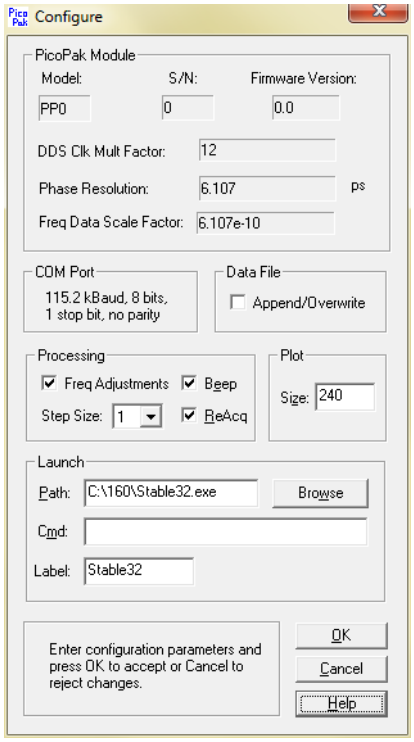


Figure 5. PicoPak Configuration Screen

The PicoPak clock measurement package also includes a Windows command line program for capturing simultaneous 10 ms data from two modules for cross-correlation analysis.

• PicoPak Clock Measurement Module Design

A complete block diagram of the PicoPak Clock Measurement Module is shown in Figure 6, and schematics of its circuits are shown in Figures 7 and 11-13. All circuits are powered from USB interface. Besides that 5V supply, the USB converter has a 3.3V regulator, and two additional 1.8V regulators supply the DDS chip. The 10 MHz reference input is split to clock the DDS, drive the 2.5 kHz divider and, via a digital comparator, provide a clock for the PIC Timer0. The signal input is buffered and connected to one input of the phase detector; it also drives a digital comparator that produces a clock for the PIC Timer1. The other phase detector input is driven by the DDS output after low pass filtration and amplification. Power is removed from both digital comparators when not needed. The phase detector output, after low pass filtration, is amplified by two op amps, one feeding the PIC ADC input and the other its analog comparator.

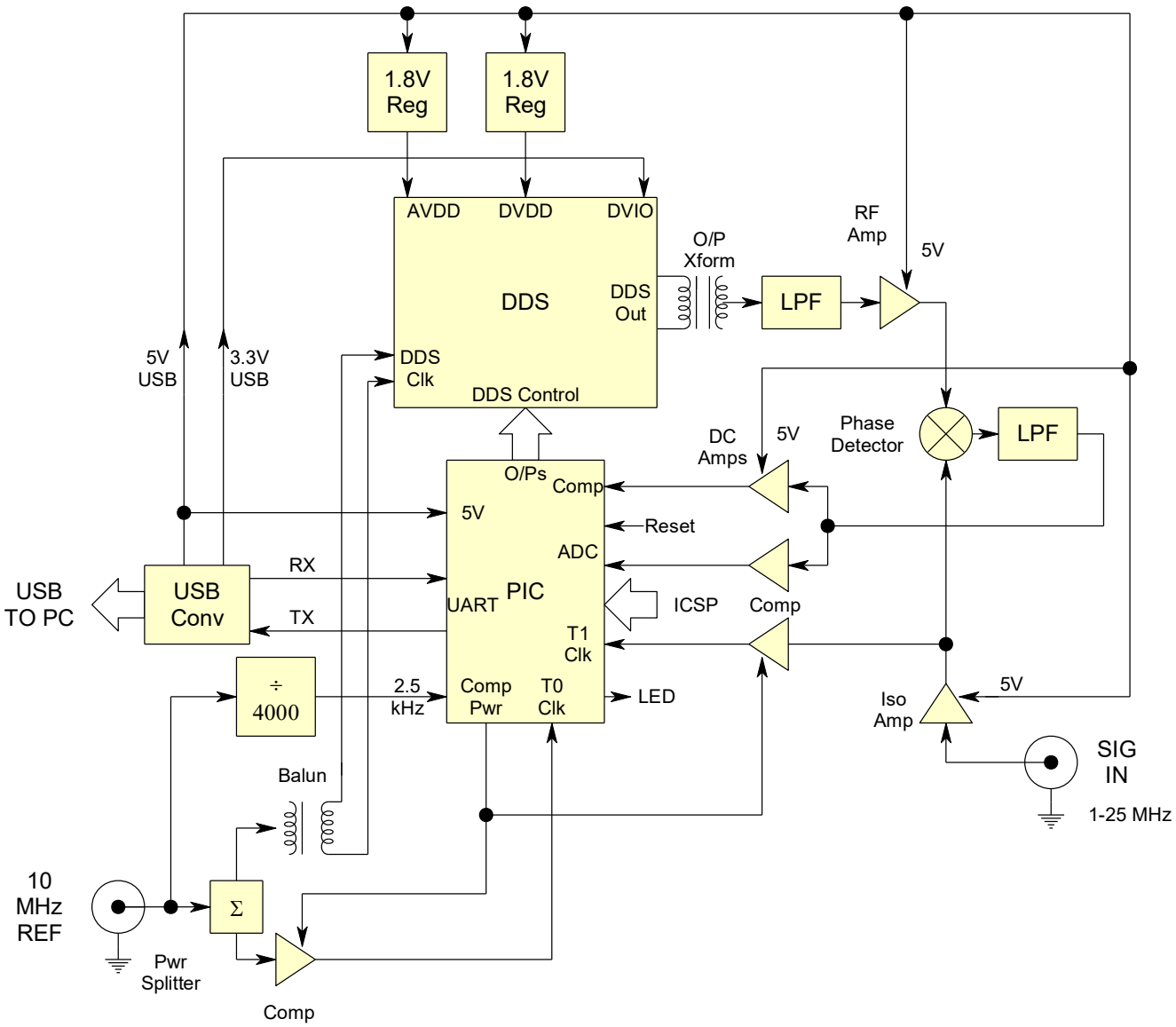


Figure 6. PicoPak Clock Measurement Module Block Diagram

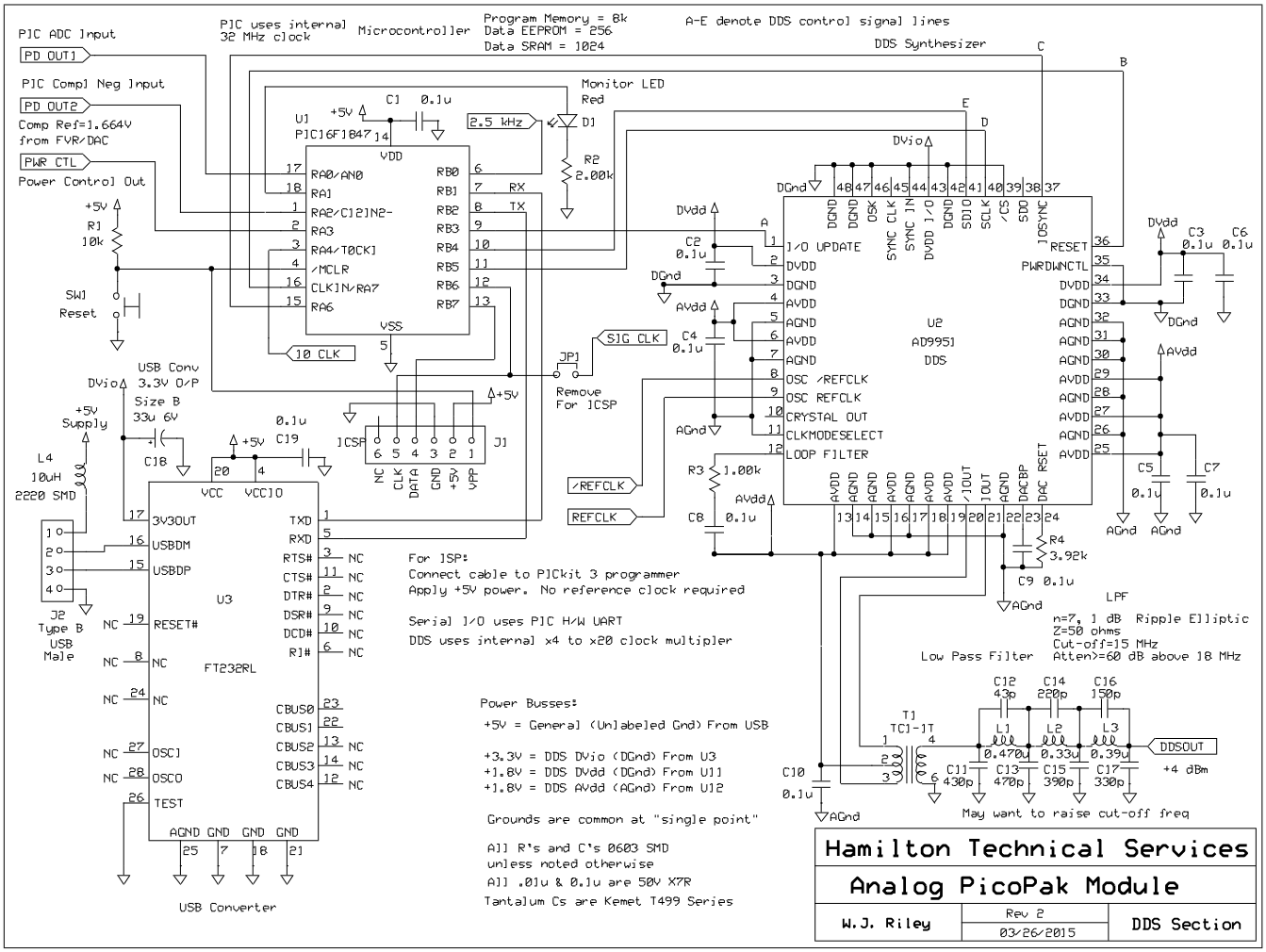
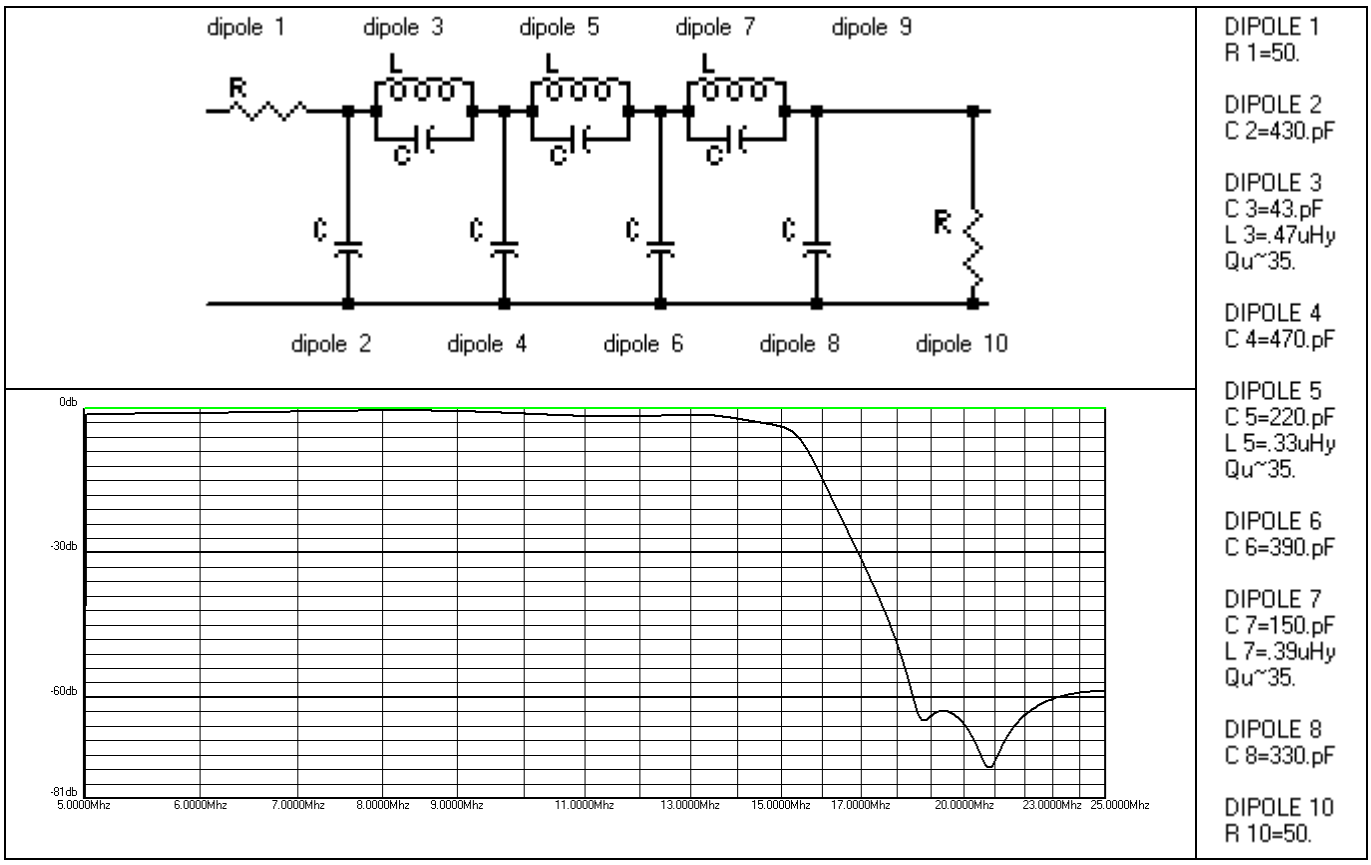


Figure 7. PicoPak Clock Measurement Module DDS Section Schematic

This section contains the DDS synthesizer with its reconstruction low pass filter, the PIC microcontroller and the USB interface converter. The PIC is programmed via its in-circuit programming (ISP) interface. A reset switch and a test LED are also included. A jumper isolates the Timer1 clock input from the ICSP interface.

The DDS reconstruction filter is a 7-section, 1 dB, 50 ohm elliptic low pass filter with a 15 MHz cut-off frequency, designed to have an attenuation of 60 dB above 18 MHz. The actual stop band attenuation, shown in Figure 8, is somewhat less but is nevertheless quite satisfactory. A higher cut-off frequency would allow the PicoPak to operate above 15 MHz.



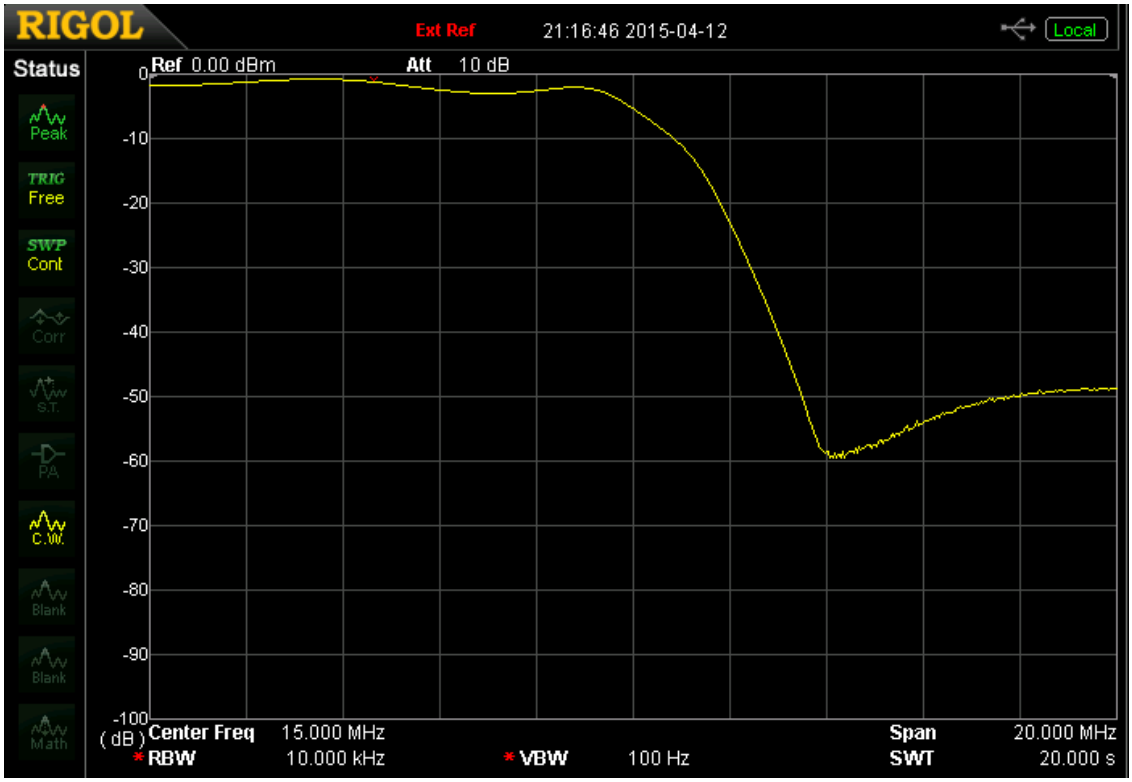
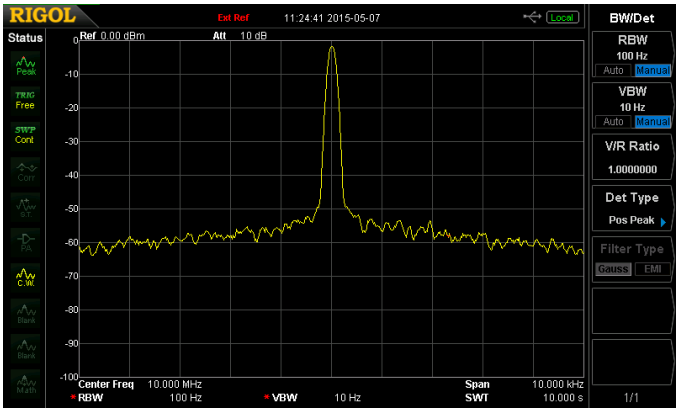
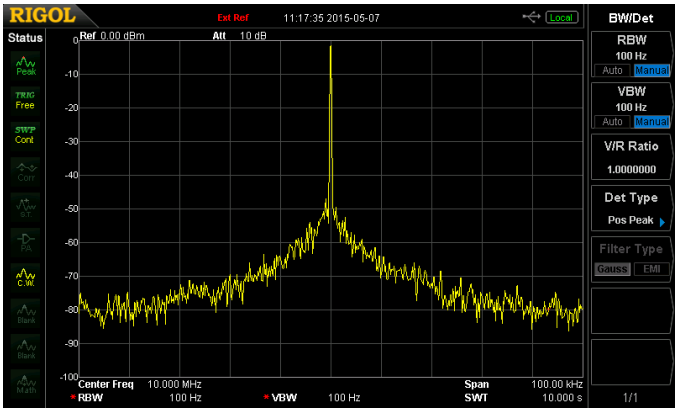


Figure 8. DDS LPF Design and Measured Frequency Response

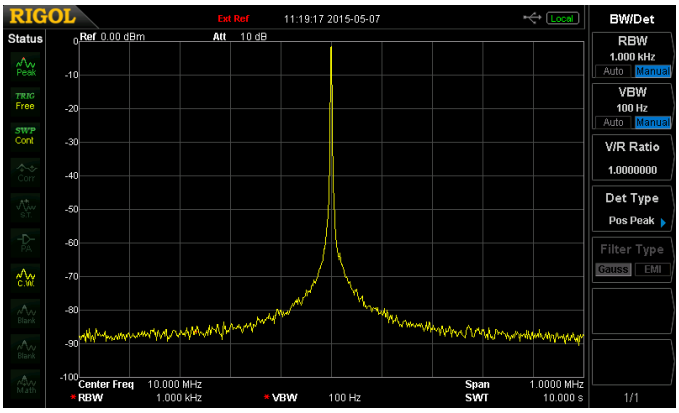
Figure 9 shows spectral plots of the DDS output at 10 MHz for spans of 10 kHz, 100 kHz, 1 MHz and 25 MHz. No spurious components are visible, there is no obvious noise pedestal near the carrier, and the 2nd harmonic is suppressed by about 60 dB. The spectrum did not change over a range of 15 dB below the nominal +7 dBm reference input level.



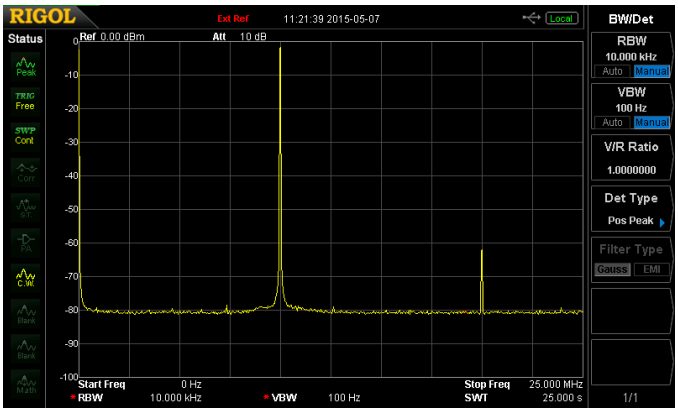
Span=10 kHz



Span=100 kHz



Span=1 MHz



Span=25 MHz

Figure 9. DDS Spectral Plots at 10 MHz

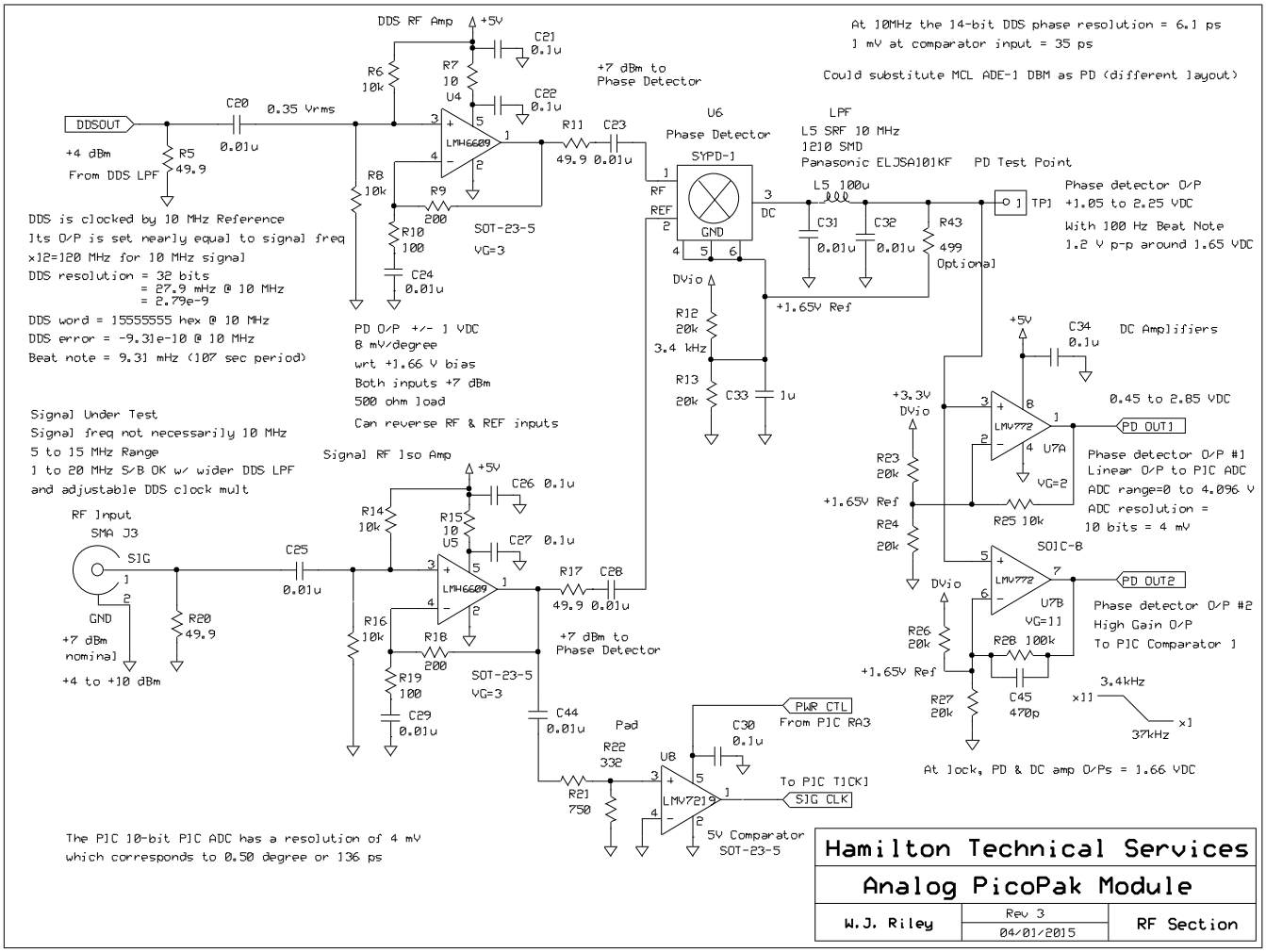


Figure 10. PicoPak Clock Measurement Module RF Section Schematic

The RF section contains RF amplifiers for the signal under test and reference signals, the phase detector and its low pass filter, two DC amplifiers and the signal comparator. The phase detector and DC amplifiers are biased at +1.65 VDC (as is the PIC analog comparator). A test point is provided for the phase detector output.

Figure 11 shows the ≈ 1.65 VDC, 1.2 V p-p waveform at the phase detector test point for a 100 Hz beat note. The scales are 200 mV/div vertical and 2.5 ms/div horizontal. This signal is amplified x2 to the PIC ADC input and x11 to its DC comparator input. The latter is a 5V p-p quasi-squarewave with the 100 Hz beat note. During normal operation, the phase detector output has a small DC level with respect to its bias voltage that represents the departure of the signal phase from exact quadrature with the DDS reference output.

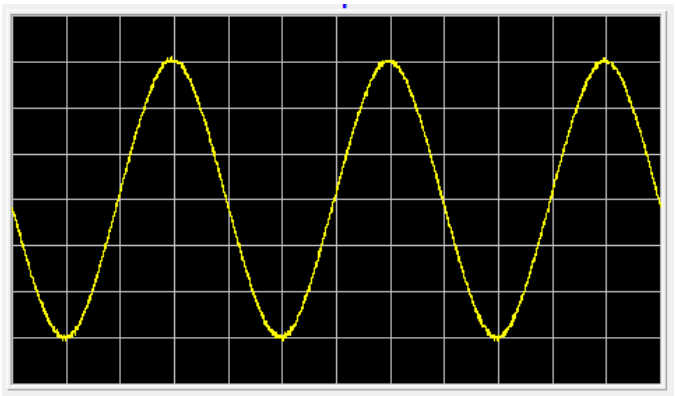


Figure 11. Phase Detector Test Point Waveform

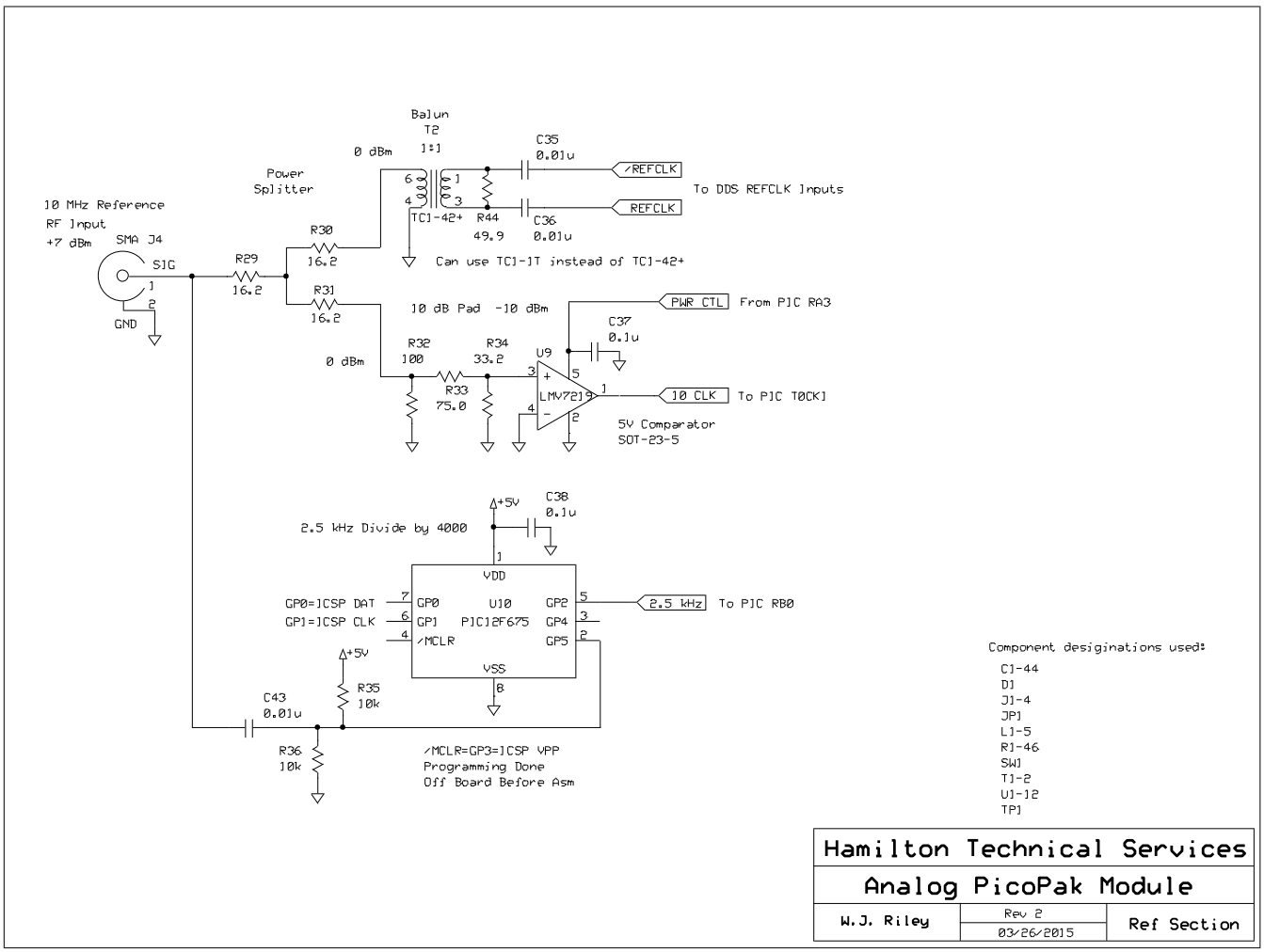


Figure 12. PicoPak Clock Measurement Module Reference Section Schematic

The reference section accepts a 10 MHz sinewave signal at a nominal level of +7 and splits it to clock the DDS differentially, provide a reference squarewave to the PIC Timer0 input, and drive another PIC device that divides it by 4000 to produce a 2.5 kHz coherent sampling rate.

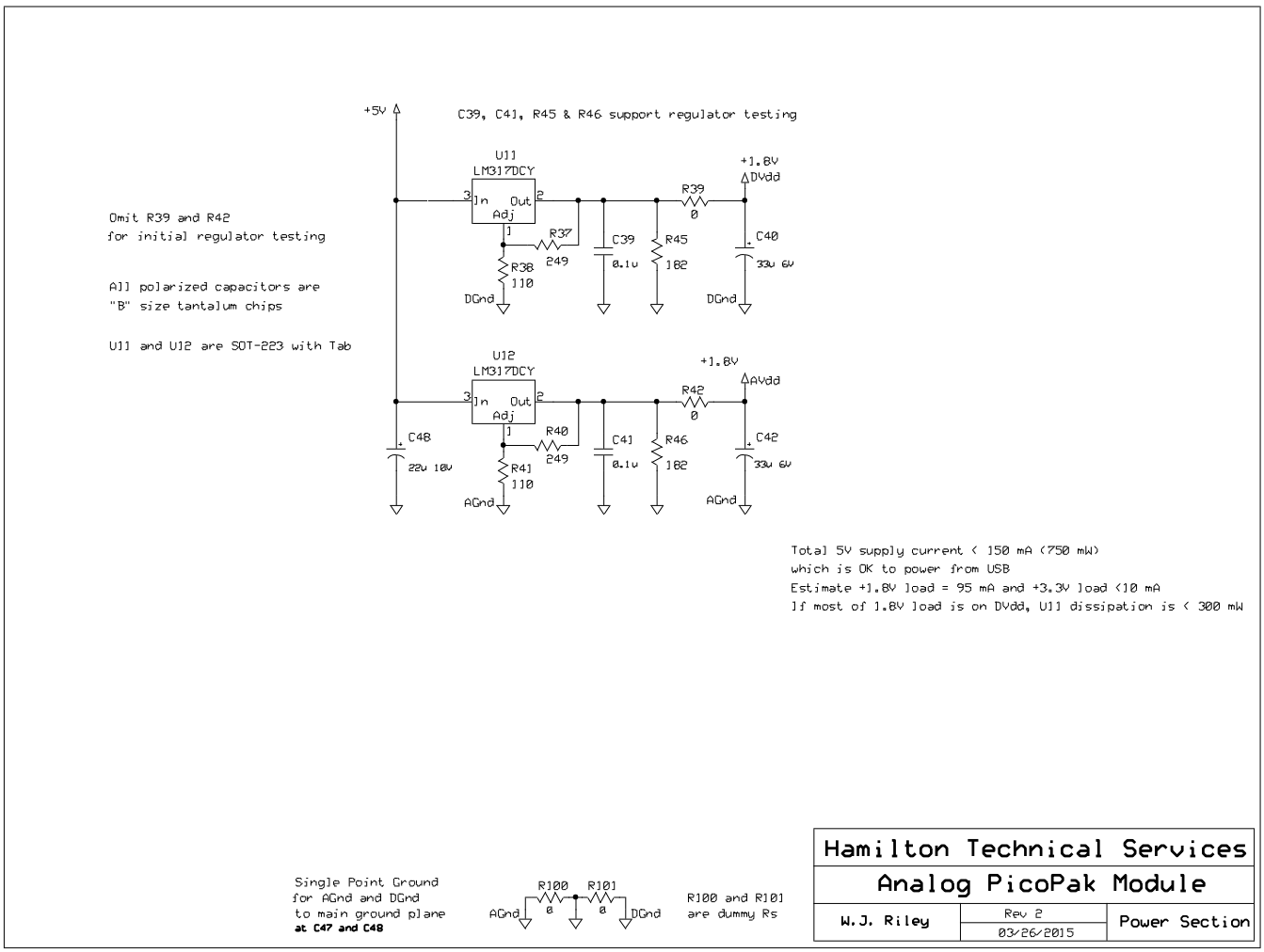


Figure 13. PicoPak Clock Measurement Module Power Section Schematic

The power section contains two +1.8 V linear regulators for the DDS DVdd and AVdd supplies.

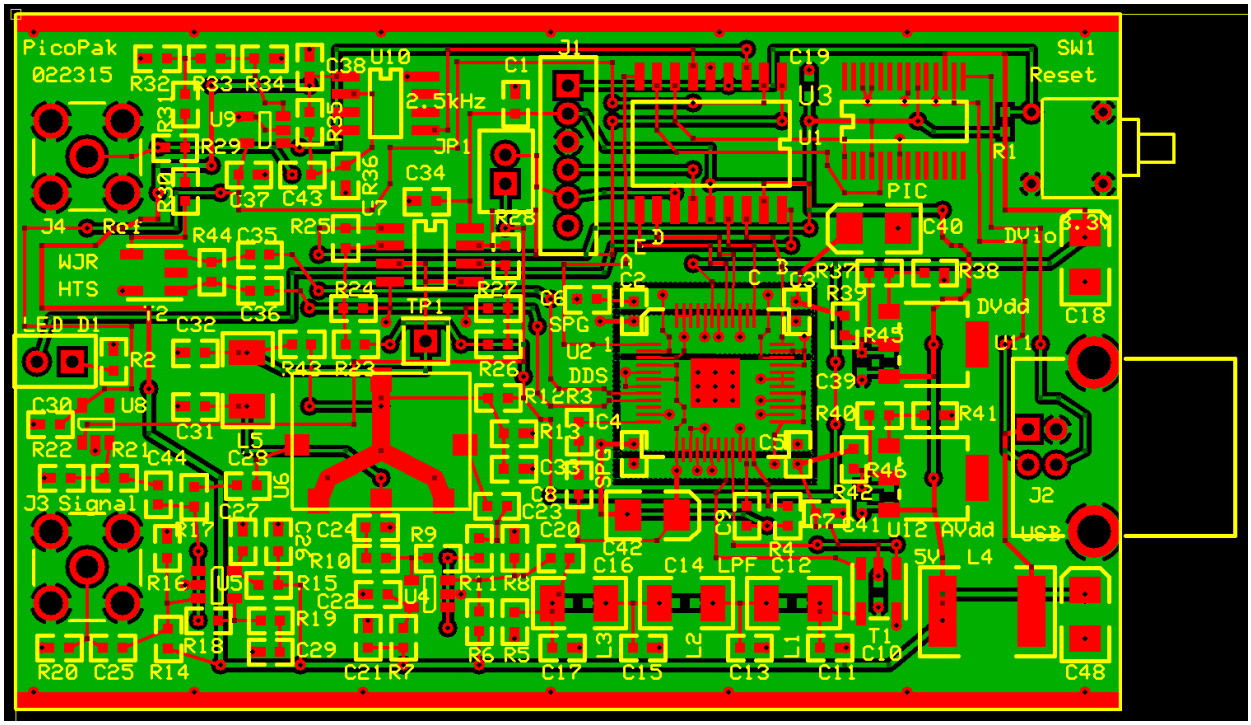


Figure 14. PicoPak Clock Measurement Module Board Layout

The module is implemented on a 2-sided 80 mm x 50 mm PCB board with solder mask and silk screen as shown in Figure 14. The ground plane beneath the AD9951 DDS chip near the center is divided into DVDD, DGND, AGND and AVDD sections. The reference and signal input SMA connectors and monitor LED are at the left edge (front) and the USB connector and reset pushbutton are at the right edge (rear). The device at the left center with the wide inverted-Y trace is the SYPD-1 phase detector. Most passives are 0603 SMDs, and a few are located on the bottom of the board.

- **DDS Control**

The PicoPak AD9951 DDS device is controlled by the PIC16F1847 via five signal lines as shown in Figure 7 and Table II.

Table II DDS Control Signals

DDS Signal	Label	PIC Pin	DDS Pin	Remarks
RESET	B	RA7 - 16	36	Resets entire DDS
IO SYNC	C	RA6 - 15	37	Synchronizes serial I/O interface
SDIO	E	RB4 - 10	41	Serial data
SCLK	D	RB5 - 11	40	Serial clock
IO UPDATE	A	RB3 - 9	1	Updates DDS data

At startup, the Reset and IO Sync lines are pulsed, the CFR2 control register is loaded by sending its 1-byte address and 3 bytes of data followed by an IO Update, and the FTW0 frequency register is loaded by sending its 1-byte address and 4 bytes of data followed by an IO Update. Each byte transfer requires 8 clock pulses. These signals are shown in Figure 15. The entire process takes about 155 µs. Similar data transfers take place during PicoPak operation.

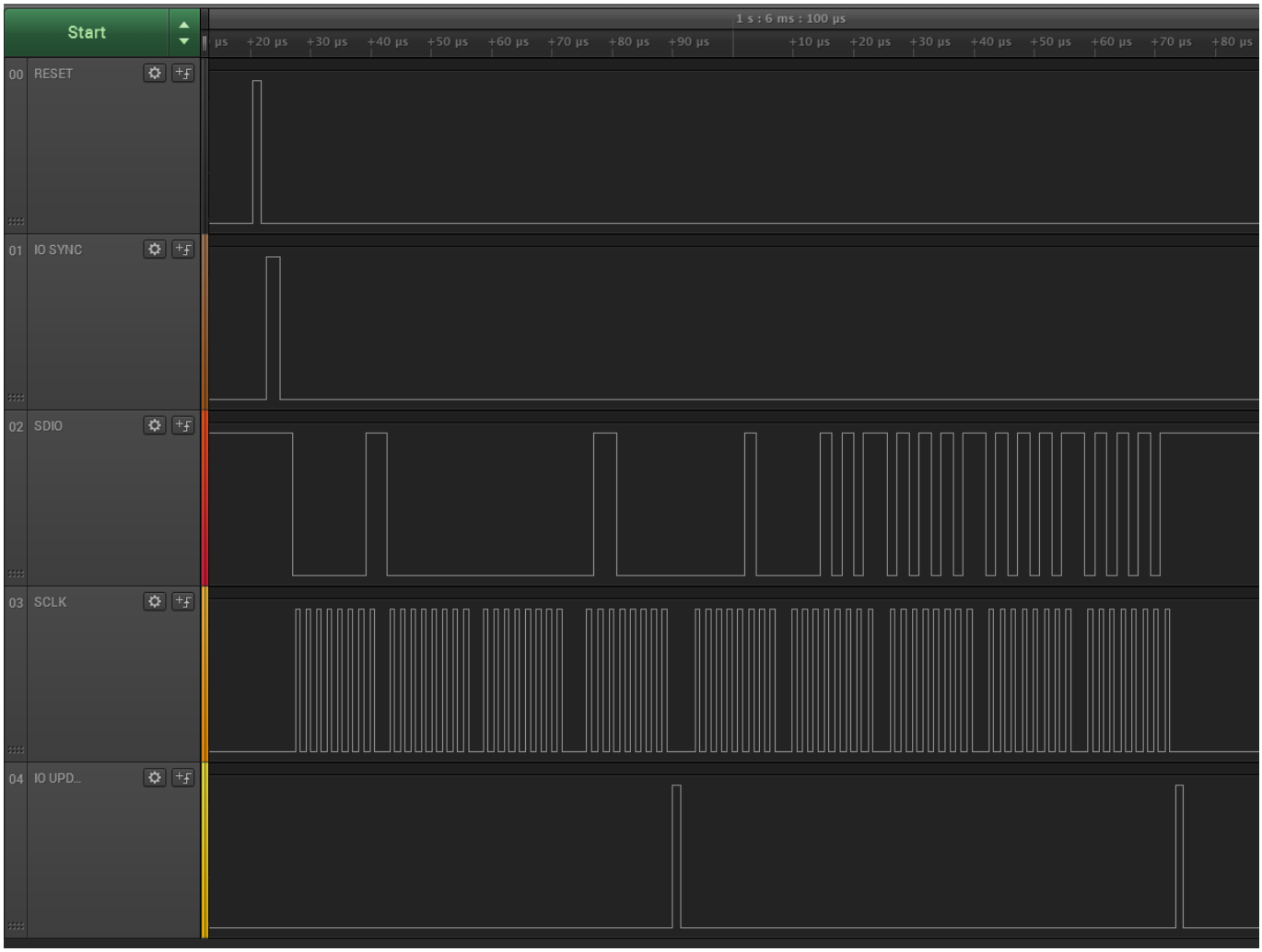


Figure 15. DDS Control Signals During PicoPak Initial Startup (DDS Word = 15555555 hex)

- **Evaluation Board Tests**

The PicoPak development began with the design, construction and evaluation of two evaluation boards, one similar to the final analog version and the second employing mainly digital circuitry. The latter offered the possibility of a simpler design but its performance was less satisfactory and an analog design was adopted. The most significant finding during the evaluation process was the need to avoid coherent phase interference generated by digital signals affecting the phase detector.

- **PicoPak Noise Floor**

The stability plot of Figure 16 is an example of a fairly long (2.7 day) coherent PicoPak measurement run that shows how its noise floor improves with longer averaging times from about 1.3×10^{-11} at 1 second down to the mid $pp10^{16}$ range at several hours.

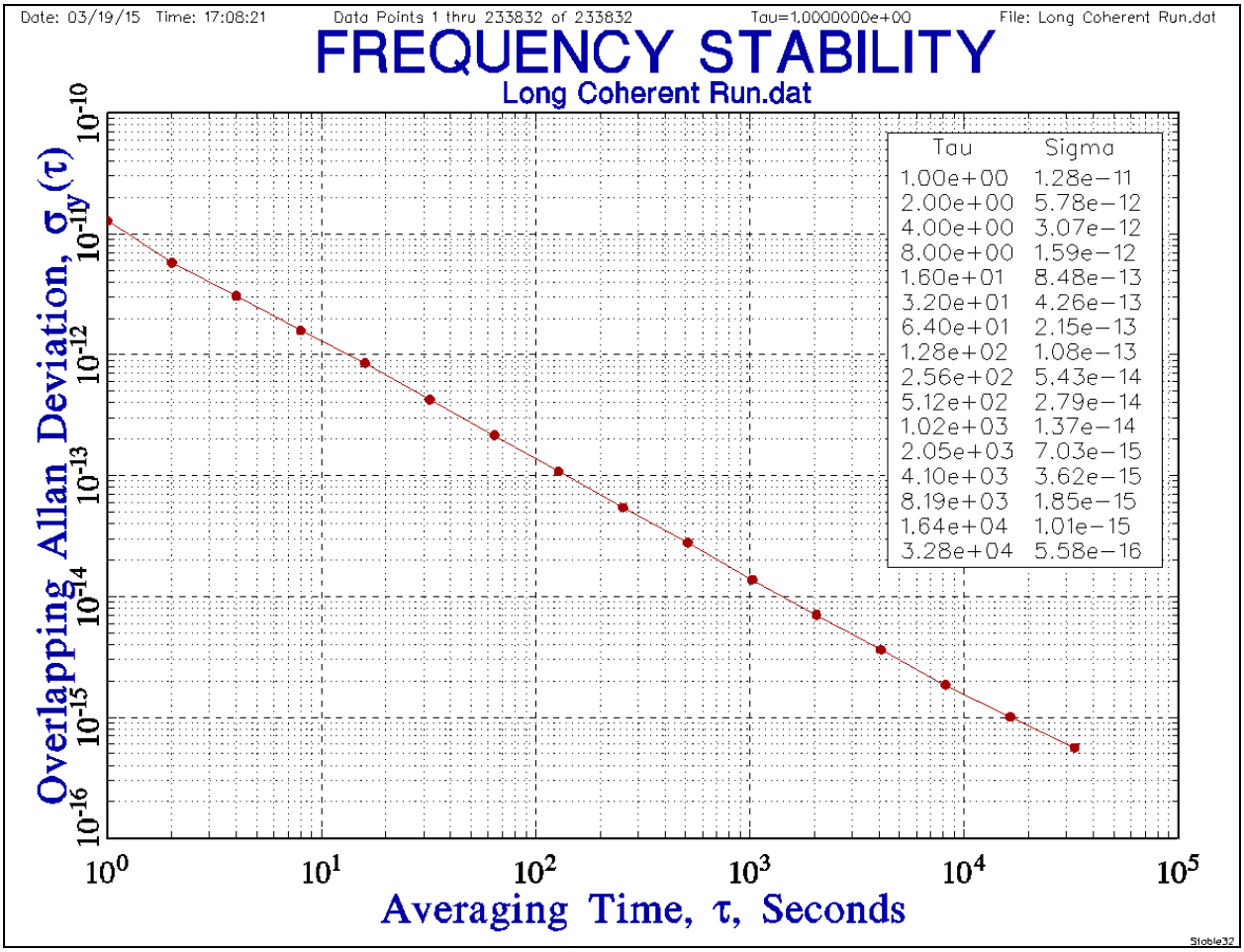


Figure 16. PicoPak Noise Floor

- **PicoPak Phase Response**

A simple verification of the PicoPak phase response is to vary the length of its signal line with a coaxial phase trimmer such as the Bracke Mfg. BM12000 shown in Figure 17. That device is a variable 50Ω coax line whose phase response was calibrated with a VNA as 1.69 ps/turn as shown in Figure 18. The measured response is exactly that expected for an air line.

Figure 17 Phase Trimmer

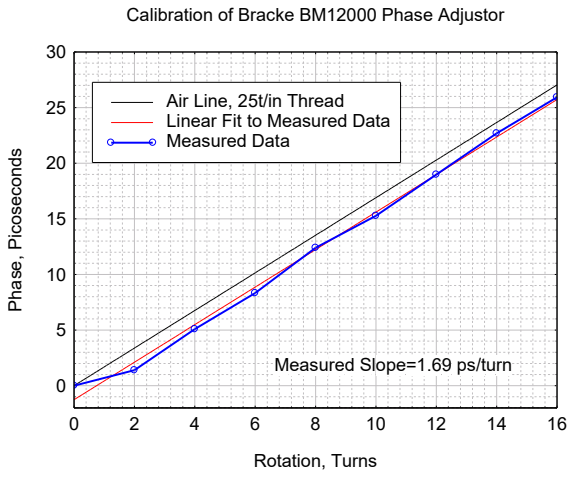


Figure 18 Phase Response

The response of PicoPak module S/N 103 to the same 16 turn phase adjustment is shown in Figure 19. A phase change of 27.3 ps was observed, in agreement with the expected value of 27.0 ps. This test is not intended to calibrate the PicoPak, since its phase sensitivity is determined exactly by the period of the signal frequency and the DDS resolution, but rather as a simple way to verify its basic response. The measured phase responds smoothly to the change in transmission line length and the noise allows phase changes on the order of 5 ps to be resolved.

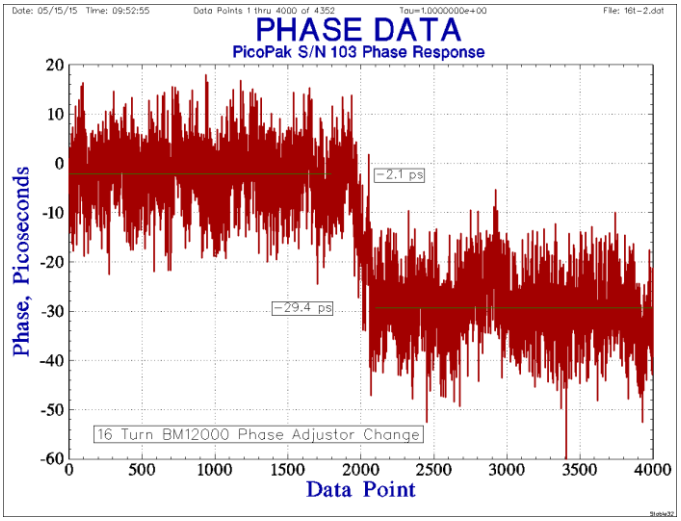


Figure 19. PicoPak Response to Phase Change

- **Phase Slew Test**

A phase slew test was conducted on PicoPak S/N 103 with coherent 10 MHz inputs and the signal frequency slightly offset to produce a linear phase slew of +0.83867 ps/s. The frequency offset was produced by using a 48-bit DDS synthesizer with a 120 MHz internal clock set to 155555555569 hex. The resulting 2.5 day phase record, shown in Figure 20, was linear, glitch-free and had very close to the expected slope (8.3779e-13) and average frequency (8.3817e-13), thus verifying the PicoPak scale factor. The small error is mainly due to PicoPak noise and temperature sensitivity.

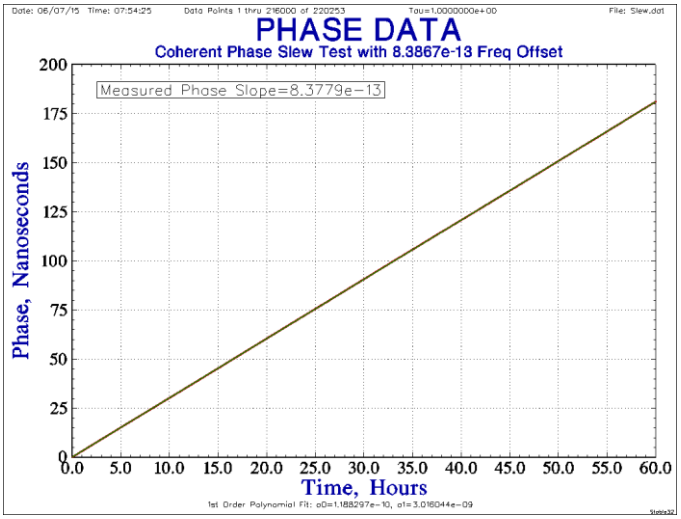


Figure 20. PicoPak Phase Slew Test

- **PicoPak Module Packaging**

The PicoPak DDS clock measurement module is a cigarette pack sized, picosecond-level clock measurement device module using a PIC microcontroller implemented on a 50 mm by 80 mm board housed in a small 3.28” x 2.25” x 1.03” Hammond 1455C801 enclosure as shown on Figures 21 and 22. It has reference and signal SMA RF connectors and a monitor LED on the front and a Type B USB connector and reset switch on the rear. It emits a phase data stream under the control of a PC user interface application and is compatible with the Stable32 and TimeLab programs for frequency stability analysis.

Figure 21. PicoPak Module Board

Figure 22. PicoPak Module Enclosure

The complete PicoPak clock measurement system includes the PicoPak module, a Type A/B USB cable and a CD-ROM that contains its Windows® GUI and command line user interface programs and associated documentation, as shown in Figure 23.

As of this writing, it remains uncertain whether or not the PicoPak clock measuring system will become a product, and, if so, in what form (assembled and tested, kit or design information) it may be made available.

Figure 23. PicoPak System Components

• Conclusions

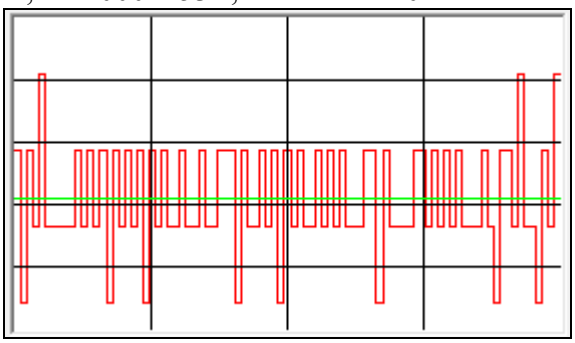
The PicoPak is a new type of clock measurement device offering moderately high precision in a small, USB-powered and low cost instrument. Its resolution and noise is comparable to that of a high-resolution interpolating time interval counter, approximately 10 ps (11 digits) per second. It measures incremental rather than absolute phase, and therefore tracks the relative phase evolution of the device under test without spillovers at the carrier period. It operates from sinusoidal RF frequencies rather than 1 pps pulses, from 5 to 15 MHz in its current form, and can track frequency changes up to $1x10^{-8}$/s, which is sufficient for most precision and semi-precision sources. The PicoPak DDS-based clock measurement technique offers an attractive alternative to traditional clock measurement methods.

• References and Notes

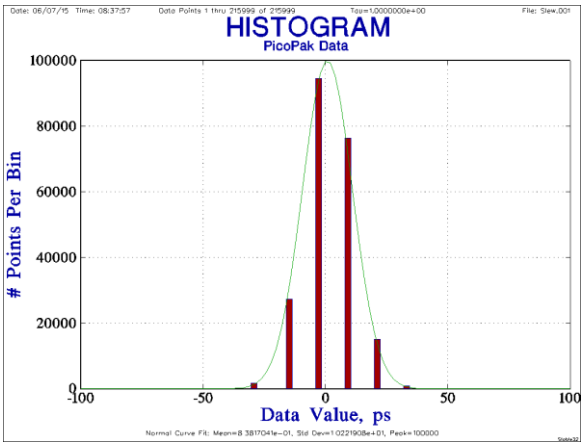
1. Private communication, T. Van Baak to W.J. Riley, PTTI Meeting, December 2, 2014.
2. D.A. Howe, D.W. Allan and .A. Barnes, “Properties of Signal Sources and Measurement Methods”, Section 8.1 The Loose Phase-Locked Loop, *Proceeding of the 35 Annual Symposium on Frequency Control*, May 1981.
3. F.M. Gardner, *Phaselock Techniques*, John Wiley & Sons, 2nd Edition, 1979, ISBN 0-471-04294-3.
4. 25 +1 or –1 phase detector readings are summed during each 10 ms data stream interval, which can produce only odd values between -25 to +25. Thus, if they alternate, the phase data produce a

squarewave with a p-p amplitude of 2, which has an rms value of 1 LS DDS phase bit, 6.1 ps at 10 MHz.

5. Data Sheet, AD9951 400 MSPS 14-Bit, 1.8 V CMOS Direct Digital Synthesizer, Analog Devices, Inc., D03359-0-5/09(A), May 2009.
6. Data Sheet, PIC16F1847, Microchip Technology, Inc., DS40001453E, November 2012.
7. If the PicoPak were noiseless, its incremental phase data would be a squarewave with a peak-to-peak amplitude of twice the DDS phase resolution, 12.2 ps at 10MHz, which has an rms value of $E_{pp}/2$ or 6.1 ps (6.1×10^{-12} at 1s). Noise causes the incremental phase data to resemble a "random telegraph signal" and increases the amplitude of some of the variations. The data must also reflect the DDS and signal frequency offsets.



That is what is seen in actual practice (see figure above), with some fraction of the readings having double the amplitude and very few more than that as shown in the histogram at right. Noise is caused by that of the signal and reference sources, DDS phase jitter (especially its clock multiplier), phase detector amplifier input noise, and comparator input noise and hysteresis. Additional noise can be caused by internal quasi-coherent interference, ground ripple and the like, as well as power supply noise.



The best $\sigma_y(\tau=1s)$ observed is about 8×10^{-12}, with 1.2×10^{-11} typical and $<1.5 \times 10^{-11}$ specified. The noise is lowest with a somewhat lower than nominal ≈ +3 dBm signal level.

8. Note added 08/12/16: I happened upon a short 2003 paper today describing an early (mid-1990's) embodiment of DDS-based phase measurement hardware very similar to the PicoPak, M. Torres, "A Very High Resolution Phase Meter for Path Stabilization". That device was used to stabilize the phase delay of a coaxial cable path used in an interferometer. The main difference, other than the older, more complex hardware, was the inclusion of an integrator between the phase detector and the comparator, thus making it a 2nd order control loop. Besides eliminating static phase error at the phase detector, making the loop dynamics more oscillatory and probably requiring a lag-lead digital loop compensator, this change would also, with a long integrator time constant, have the effect of making the phase readings resemble those of a modified Allan deviation because of the additional phase integration. The cited IRAM French mm-wave radio astronomy application was not for phase measurements per se, but rather a phase stabilization system. The paper shows phase data having a noise level on the order 0.01 degrees p-p at 1.8 GHz, equivalent to about 16 fs p-p. This extremely high resolution was largely the result of heterodyning the 1.8 GHz signal down to 500 kHz, where the baseband resolution is about 56 ps p-p or about 18 ps rms, somewhat larger than that of the PicoPak but, of course, including the noise of the source and downconverter (the IRAM used a 32-bit DDS with 17 bits or 2.5 millidegrees of phase resolution).

Appendix I

PicoPak Clock Measurement Module Specifications			
Parameter			**Specification**
Signal Input	Frequency		5 to 15 MHz
	Waveform		Sinusoidal
	Level		0 to +10 dBm
	Impedance		50 ohms nominal
	VSWR		≤ 1.5:1 between 5 to 15 MHz
Reference Input	Frequency		10 MHz
	Waveform		Sinusoidal
	Level		0 to +10 dBm
	Impedance		50 ohms
	VSWR		≤ 1.5:1 at 10 MHz
Resolution	Phase		0.022 degrees at signal frequency (6.1 ps at 10 MHz)
	Frequency		$1x10^{-11}$ at 1 second (11 digits/s)
Noise	0.01-10,000 seconds (or longer)		≤ $3x10^{-11}/\tau$, ≤ $1.5x10^{-11}/\tau$ typical , for τ in seconds
	Floor		≤ $1x10^{-15}$ (or lower)
Frequency Accuracy	Coherent Phase Slope		≤ $1x10^{-15}$ (or lower), low $pp10^{16}$ typical for long averages
Frequency Slew	Tracking Limit		≤ $1x10^{-8}$/second
Temperature Coefficient	Phase versus Temperature		+5 ps / °C typical
O/P Data Stream (uses standard FTDI PC USB to serial port driver)	Sampling Rate		2.5 kHz (τ=400 μs)
	Proprietary documented formats, ASCII characters, 1 row per datum, no timetags	#1 @ 100 Hz rate	Numeric values of the incremental frequency variations in units of 100 signal periods in seconds divided by 2^{14} ($6.1x10^{-10}$ at 10 MHz)
		#2 @ 100 Hz rate	Hex values representing the incremental phase and frequency variations
		#3 @ 1 Hz rate	Hex values representing the incremental phase and frequency variations and phase corrections for frequency adjustments
	Proprietary binary documented format	#4 @ 100 Hz rate	1 byte (char) w/o CR/LF representing signed incremental phase variations
USB Commands	Alphabetic ASCII Characters		Proprietary documented commands to control PicoPak from PC
Power	Voltage		5 VDC from USB
	Current		≤ 100 mA (85 mA typical)
Connectors	USB		Type B Male on rear panel
	Signal Input		SMA Female on front panel
	Reference Input		SMA Female on front panel
	Programming		Internal 6-Pin 2 mm header for Microchip PICkit-3 (factory use only)
Indicators	Monitor		LED on front panel
Controls	Reset		Pushbutton on rear panel
Physical	Size (LxWxH)		3.28”x2.25”x1.03” (excluding connectors, feet and trim)
	Weight		≤ 5 oz (extruded aluminum case)
Accessories (Included)	Cable		5’ USB Type A plug to Type B plug with ferrite choke
	Software		PC application to control PicoPak PP1 module
	Documentation		Paper describing PicoPak design, PC application help file

Note: These specifications are preliminary and subject to change without notice